MPC5777C course description/agenda

Course Title: MPC5777C (Cobra55nm) PowerPC Multi-Core Architecture

When: Upcoming courses listed at www.ashware.com/MCU-Training-Offerings
Start Time: 9 am
Stop Time: 5 pm

Where: NXP Office
28125 Cabot Drive
Suite 100
Novi, Michigan 48377

Course Description: This 3 day course offers in-depth overview of the Multi-Core MPC5777C (Cobra55nm) device. Full coverage of the PowerPC cores is provided including Power Architecture main features, operation and Programming.

To ensure safety integrity level (ASIL) and meet ISO 26262 standards and requirements for safety critical applications, the Cobra device integrates two cores running in Lock-step with redundancy checkers for error and glitch detection along with End-to-End Error Correction Code (E2E) will be covered.

The course will cover the on-chip caches, memory management unit (MMU), system memory protection Unit (MPU), system Integration and chip pad configuration, system exception and handling, interrupt controller and external interrupts, boot assist module (BAM) and startup sequence for all on-chip processor cores.

Details of most of on-chip peripherals, such as Deserial Serial Peripheral Interface (DSPI), ZipWire / LFAST, SIPI & LVDS, CAN Bus and other serial interfaces are covered.

The Enhanced Modular I/O System (eMIOS), and the Programmable Enhanced Time Processor Unit (eTPU2+) will be covered in details with some real application examples along with the periodic interrupt timers (PITs), system timers (STMs), watchdog timers (WDGs).

It also covers the multiple on-chip RSD eQADCs and Sigma Delta SD_ADCs including decimation filter and eTPU reaction channels.

After completing the course, the participant will understand the basic concept of the MPC5777C device and all its major functional blocks.

Details Agenda:
Day 1

MPC5777C Overview

- Road Map
- Architectural features
- Two cores running in lock-step
- Internal buses and End-to-End ECC
- Redundancy and checkers
- Multi-masters and cross bar switch
- Core programming Model (e200z7 Core)
- Classic PowerPC Instruction Set
- Signal Processing Engine
- Core Exceptions and I/O Interrupts
- Interrupt Controller
- Context Switching (New Instructions)
- Dual Core basic operation and Programming
- Semaphore unit (SEM4)
- Memory Management Unit (MMU)
- System Caches
- Memory Protection Unit

Day 2

Clock Generation and Initialization

- PLL and System Clock Generation
- Pad (Pin) Assignment and Configuration
- Boot-assist Module (Boot Sequence) Device Configuration
- System Reset Sources and Reset Handling
- Software Initialization Checklist after Power-on and Resets

System Timers

- Enhanced DMA (eDMA2)
- Software Watchdog Timer (SWT)
- System Timers (STM)
- Periodic Interrupt Timers (PIT)
- Enhanced Modular I/O System (eMIOS200)
- Enhanced Timer Processor Unit (eTPU2+)

Day 3

Peripherals

- Queued A/D Converter (eQADC)
- Sigma-Delta ADC (SDADC)
- Decimation Filter
- eTPU Reaction Module
- Enhanced Serial Communication Interface (eSCI) and LIN Bus
- Deserial-Serial Peripheral Interface (DSPI)
- CAN Bus (FlexCAN2 Module)
- ZipWire

System Memory

- Error Correction Code
- SRAM Operation
- Flash Erase and Programming Sequence
- PASS Security and Tamper Detection
- CRC module
- Built In Self-Test
- Functional Safety

Tools

- Nexus Summary
- Calibration

Who Should Attend: Software and system engineers who need to come up to speed quickly on how to program and design with the MPC5777C Device.

Prerequisite: Knowledge/experience of some microprocessor/microcontroller is necessary.

Course Fee: USD$1500 per participant

Note: Breakfast and Lunch will be provided daily