**MPC5777C course description/agenda**

**Course Name:** MPC5777C (Cobra55nm) PowerPC Multi-Core Architecture

**When**: September 25-27/2018 Start Time: 9:00 AM
Stop Time: 5:00 PM

**Where**: NXP Office.
Novi, Michigan

**Target Applications:** Automotive, aerospace, and industrial.

**Course Description:** A&M in cooperation with NXP will be offering a 3 day in-depth overview of the Multi-Core MPC5777C (Cobra55nm) device. Full coverage of the PowerPC cores is provided, including Power Architecture main features, operation and Programming.

To ensure safety integrity level (ASIL) and meet ISO 26262 standards and requirements for critical applications, the Cobra55 device integrates two cores running in Lock-step with redundancy checkers for error and glitch detection along with End-to-End Error Correction Code (E2E) will be covered.

The course will cover the on-chip caches, memory management unit (MMU), system memory protection Unit (MPU), system Integration and chip pad configuration, system exception and handling, interrupt controller and external interrupts, boot assist module (BAM) and startup sequence for all on-chip processor cores.

Details of most of on-chip peripherals, such Deserial Serial Peripheral Interface (DSPI), eDMA engine, serial interfaces, periodic interrupt timers (PITs), system timers (STMs), watchdog timers (WDGs).
It also covers the multiple on-chip RSD eQADCs and Sigma Delta SD_ADCs including decimation filter and eTPU reaction channels.
The Enhanced Modular I/O System (eMIOS), and the Enhanced Time Processor Unit (eTPU2+) with some real application examples will also be covered.

After completing the course, the participant will understand the basic concept of the MPC5777C device and all its major functional blocks.

**Details Agenda:**

**Day 1**

**MPC5777C Overview**

- Road Map
- Architectural features
- Two cores running in lock-step
- Internal buses and End-to-End ECC
- Redundancy and checkers
- Multi-masters and cross bar switch
- Core programming Model (e200z7 Core)
- Classic PowerPC Instruction Set
- Signal Processing Engine
- Memory Management Unit (MMU)
- System Caches
- Memory Protection Unit
- Semaphore unit (SEM4)
- Core Exceptions and I/O Interrupts
- Interrupt Controller
- Context Switching (New Instructions)

**Day 2**

**Clock Generation and Initialization**

- PLL and System Clock Generation
- Pad (Pin) Assignment and Configuration
- Boot-assist Module (Boot Sequence) Device Configuration
- System Reset Sources and Reset Handling
- Dual Core basic operation and Programming
- Software Initialization Checklist after Power and Resets
- Enhanced DMA (eDMA2)

**System Timers**

- Software Watchdog Timer (SWT)
- System Timers (STM)
- Periodic Interrupt Timers (PIT)
- Enhanced Modular I/O System (eMIOS200)
- Enhanced Timer Processor Unit (eTPU2)

**Day 3**

**Peripherals**

- Queued A/D Converter (eQADC)
- Sigma Delta ADC (SDADC)
- Decimation Filter
- Reaction Module
- Enhanced Serial Communication Interface (eSCI) and LIN Bus
- DSPI
- FlexCAN2 and CANFD

**System Memory**

- Error Correction Code
- SRAM
- Flash Erase and Programming
- PASS Security and Tamper Detection
- CRC module
- Built In Self-Test
- Functional Safety

**Tools**

- Nexus Summary
- Development Trigger Semaphores
- Calibration

**Who Should Attend:** Software and system engineers who need to come up to speed quickly on how to program and design with the MPC5777C Device.

**Prerequisite:** Knowledge/experience of some microprocessor/microcontroller is necessary.

**Course Fees:** $1500.00 per participant

Fees are to be negotiated when training is delivered at customer's site.