MPC5746M & MPC5777M course description/agenda

Course Title: MacKinley/Matterhorn PowerPC Multi-Core Architecture

When: October 14-17
Where: Freescale Semiconductor
28125 Cabot Drive, Suite 100
Novi, Michigan 48377

Target Applications: Automotive, aerospace, industrial, and commercial.

Course Description: This 3 day course offers in-depth overview of the Multi-Core MPC5746M and MPC5777M devices. Full coverage of the on-chip PowerPC cores is provided including Power Architecture main features, operation and Programming.

To ensure safety integrity level (ASIL) and meet ISO 26262 standards and requirements for critical applications, these devices integrate two cores running in Lock-step with redundancy checkers for error and glitch detection along with End-to-End Error Correction Code (E2E) will be covered.

The course covers the on-chip tightly-coupled memories including instruction and data caches, core memory protection unit (CMPU), system memory protection Unit (SMPU), Low power management, system Integration and chip pad configuration, system exception, Interrupt controller and external interrupts, boot assist Flash (BAF) and startup sequence for all on-chip processor cores, semaphore unit (SEM4) which allows sharing of system resources to ensure data integrity and coherency, cross-bar switches to support simultaneous multi-master to multi-slave accesses.

Detail coverage of most of on-chip peripherals, such Deserial Serial Peripheral Interface (DSPI), micro-second channel (TSB) and other serial interfaces, eDMA multiplexers and eDMA engine, periodic interrupt timers (PITs), system timers (STMs), watchdog timers (WDGs)

It also covers the multiple on-chip SAR_ADCs and SD_ADCs including trigger signals from GTM and other external signals.

Full details of the Generic Timer Module (GTM) also covered.
After completing the course, the participant will understand the basic concepts of the MPC5746M and MPC5777M multi-core devices and all major functional blocks.

Details Agenda:

Day 1

MPC5777 Overview
  - MPC5700 Family Roadmap
  - Main Features and System Architecture
  - On-chip tightly-coupled memories including instruction and data caches
  - Level 1 and level 2 memory organization and operation
  - Power architecture cores programming Model that covers (e200z7 and z425) cores including variable-length encoding (VLE) and light signal processing unit (LSP)
  - Core memory protection unit (CMPU)
  - Crossbar switches and bus master arbitration sequence
  - System memory protection unit (SMPU)
  - Power Architecture Exceptions and Interrupts

Day 2

Interrupt controller, architectural features and startup sequence
  - Interrupt Controller and Context Switching (New Instructions)
  - Semaphore Block
  - System Clock Generation and PLL operation
  - Pad (Pin) assignment and configuration
  - Boot-assist Flash (BAF boot sequence)
  - System Reset Sources and Reset Handling
  - Device configuration and system initialization at startup
  - Mode Entry Module (Low power and run modes)
  - DMA_Multiplexers
  - eDMA functional description and programming

Day 3
Serial Interfaces
- DSPI
- Microsecond channel (TSB)
- CRC generator
- Introduction to FlexRay

Memories, Analog and system timers
- Flash and SRAM
- Flash organization and programming
- Error Correction Code
- Software Watchdog Timers (SWT)
- System Timers (STM)
- SAR_ADGs and SD_ADC architecture and operation
- System timers (STMs), periodic interrupt timers (PITs) and watchdog

Generic Timer Module (GTM)
- Timer overview
- Timer Input Module (TIM)
- Timer Output Module (TOM)
- ARU connected Timer Out Module (ATOM)
- Basic Operation and Programming
- Angle Clock Generation and Operation
- Examples

Functional Safety
- Introduction to Functional Safety
- 2 cores running in Lock-step for safety Integrity
- Fault Control and Collection Unit (FCCU)
- Self-Test Control Unit (STCU2)
- Meeting ASIL 26262 Standards

Tools
- Nexus Summary

Who Should Attend: Software and system engineers who need to come up to speed quickly on how to program and design with the MPC57xx family.

Prerequisite: Knowledge/experience of some microprocessor/microcontroller is necessary.

Course Fees:
Fees are to be negotiated when training is delivered at customer's site.